Power stage design and optimization for low power, high frequency, integrated DC-DC converter

Florian Neveu, University of Lyon, Ampère Lab, France - Bruno Allard, INSA Lyon, Ampère Lab, France - Christian Martin, University of Lyon, Ampère Lab, France - Frédéric Voiron, IPDiA, France

Context and objectives

Abstract

This e-poster presents the design and optimization of a high switching frequency, integrated DC-DC converter. The design target is to convert 3.3 V to 1.2 V, and to supply 280 mA with 90 % efficiency. Preliminary studies are presented, including a technology and a topology evaluation. Based on the results of these studies, a converter using a cascoded power stage has been designed and optimized with a 40 nm Bulk CMOS technology.

The converter die will be flipped on a passive interposer, taking benefits from high performances passive components (trench capacitors and racetracks inductors) and very low package parasitics.

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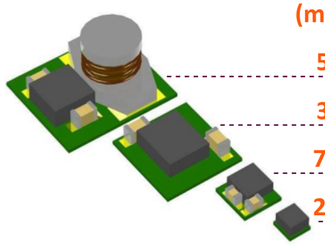
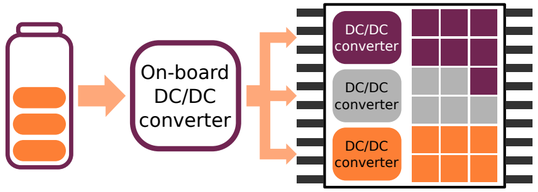
Increasing the switching frequency



Area (mm^2)	Volume (mm^3)	Frequency (MHz)
50	150	1
30	25	5
7.0	3.5	20
2.0	1.0	50-100

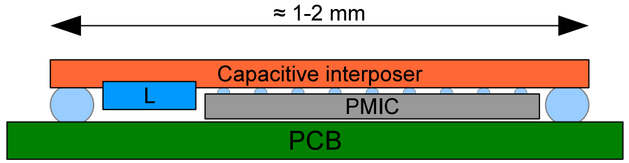
Increasing the switching frequency allows to use passive components (inductors and capacitors) with smaller values, thus reducing their footprint and height.

Simple structure of a battery-powered chip



We aim to design a converter that will be integrated inside the digital chip. It will allow a granular power management of the digital chip, and reduce the constraints of the on-board DC-DC converter.

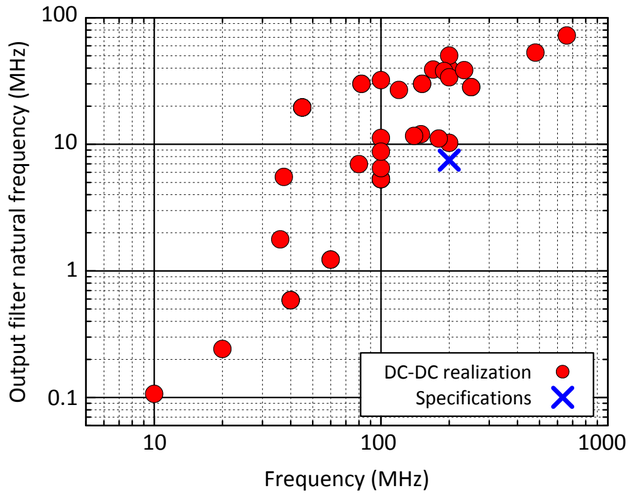
Cross-section of physical target



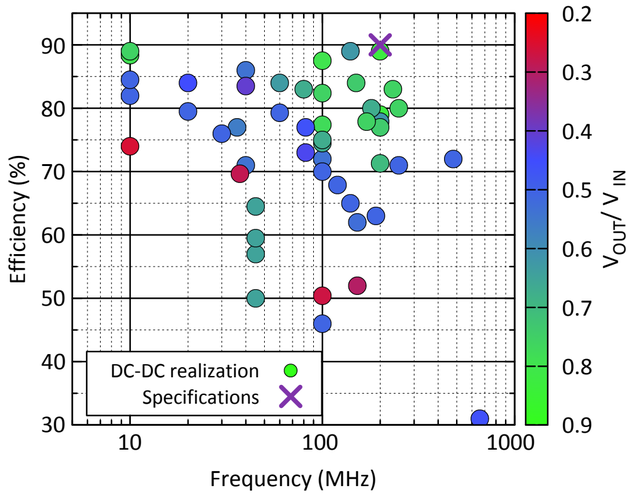
Specifications summary (nominal)

	Value	Unit
Input voltage	3.3	V
Output voltage	1.2	V
Output current	280	mA
Output power	336	mW
Output voltage ripple	± 2	%
Frequency	100 - 200	MHz
Efficiency	90	%
Active area	≤ 1	mm^2
Passive area	≤ 10	mm^2
Totale area	≤ 10	mm^2
Height	≤ 1.2	mm
Technology	40	nm

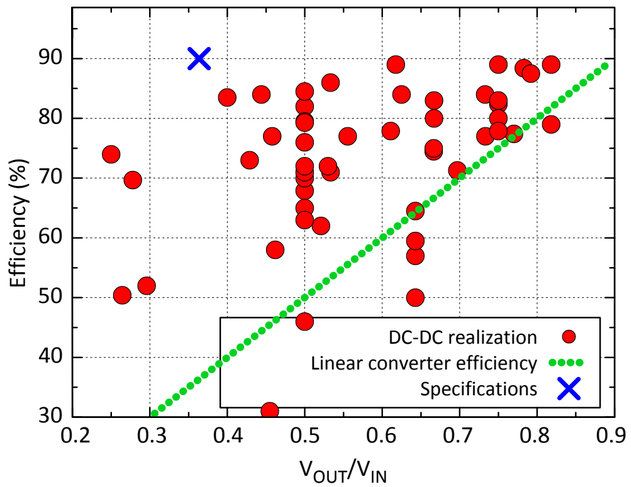
State-of-the-art - Low power, high frequency, non-isolated converters



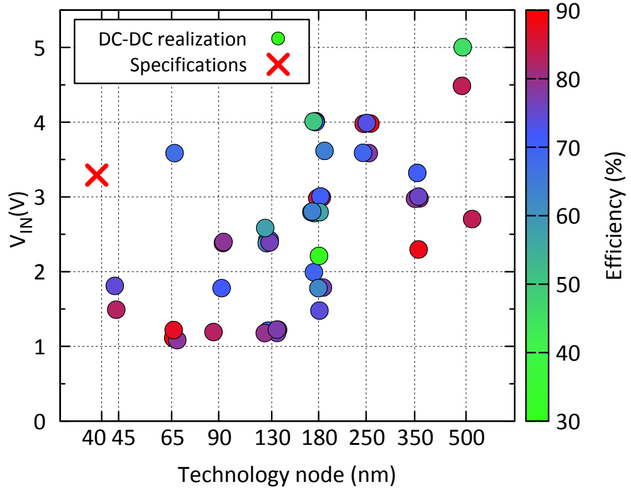
Frequency ↗ ⟹ Filter values ↘



Frequency ↗ ⟹ Efficiency ↘



Ratio ↘ ⟹ Efficiency ↘



Technology ↘ ⟹ Input voltage ↘

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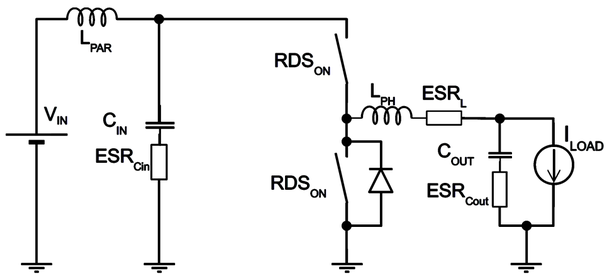
Architecture evaluation - High level analysis

Conditions de simulation:

V_{IN} = 3.3 V; V_{OUT} = 1.2 V; I_{LOAD} = 280 mA; L_{PH} = 50 nH; ESR_L = 50 mΩ; C_{IN} = 250 nF; ESR_{CIN} = 250 mΩ; C_{OUT} = 250 nF; ESR_{COUT} = 250 mΩ; RDS_{ON} = 500/1000 mΩ; F_{SW} = 200 MHz

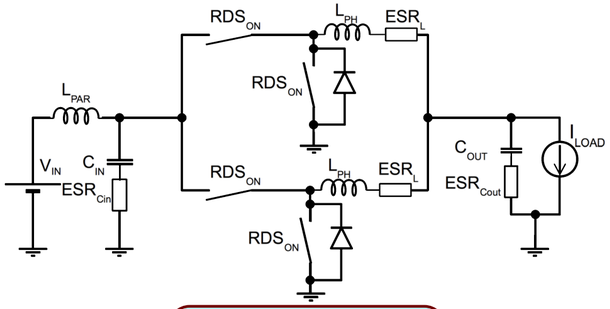
Standard buck



Efficiency: 79.4 %

Reference design

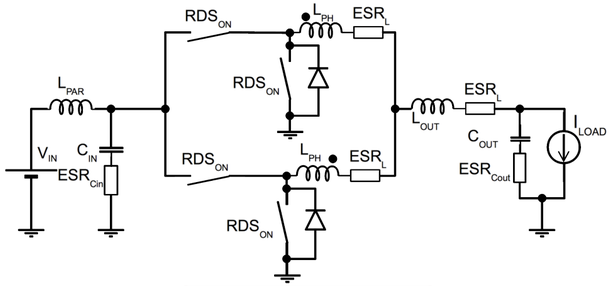
2-phases buck



Efficiency: 81.5 %

Slight improvement compared to reference

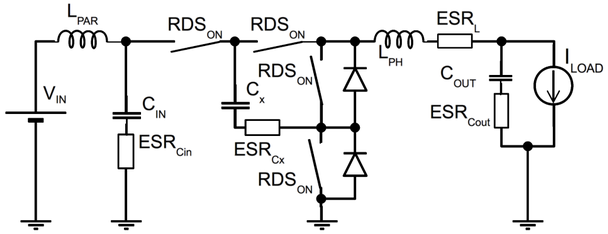
2-phases coupled buck



Efficiency: 85.5 %

Good improvement compared to reference

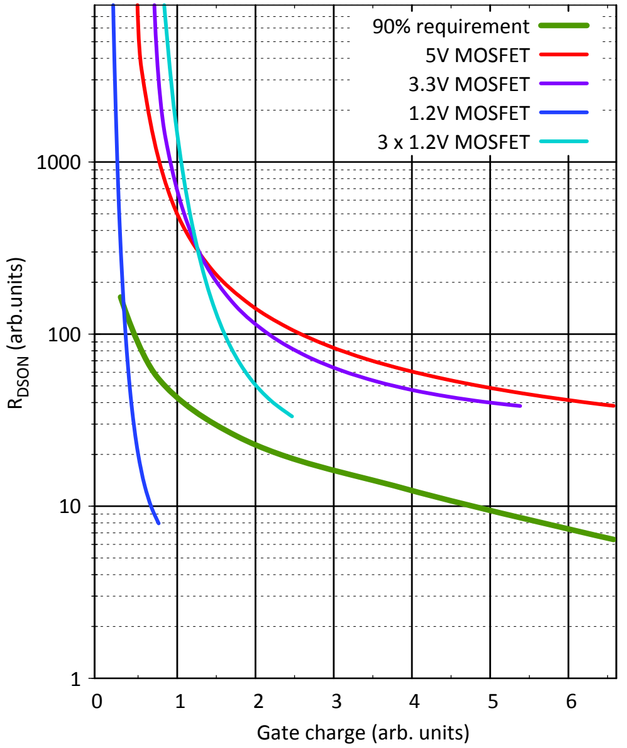
3-levels converter

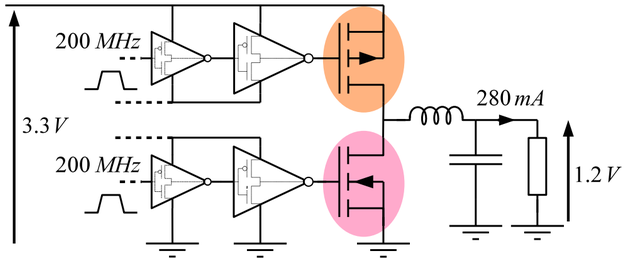


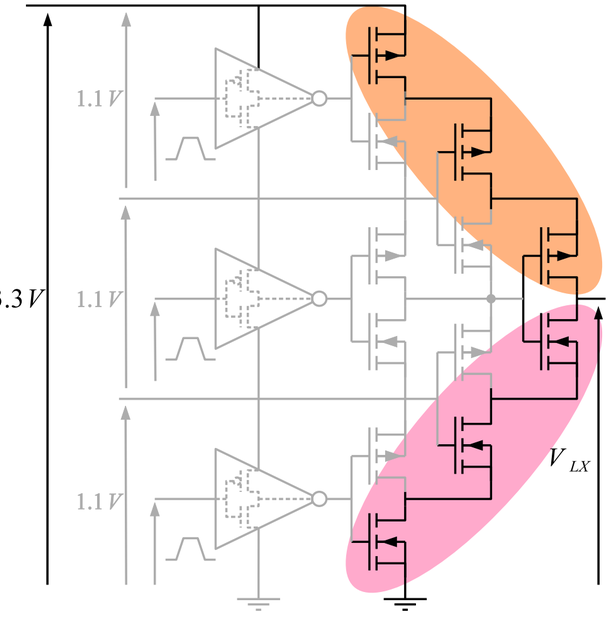
Efficiency: 69.4 %

Large degradation compared to reference

Technology evaluation







- Analysis based on R_{DSON} - Q_G FOM
- Analysis carried on nominal power point
  - 3.3 V to 1.2 V
  - 280 mA output current
  - 200 MHz switching frequency
- Assuming a standard 1-phase Buck converter
- Only steady-state is considered

Best efficiency can be achieved using low voltage devices associated in series

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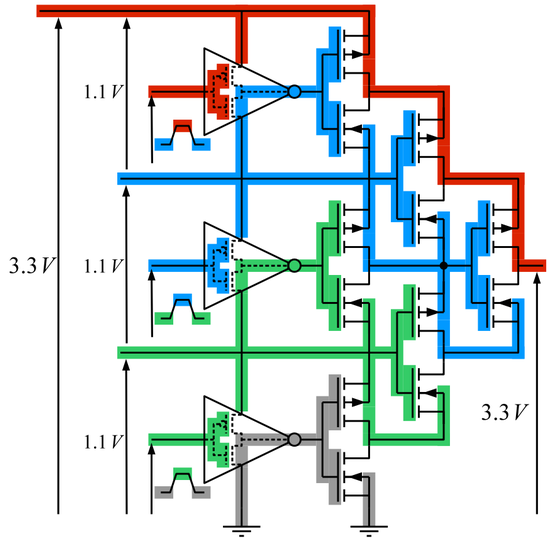
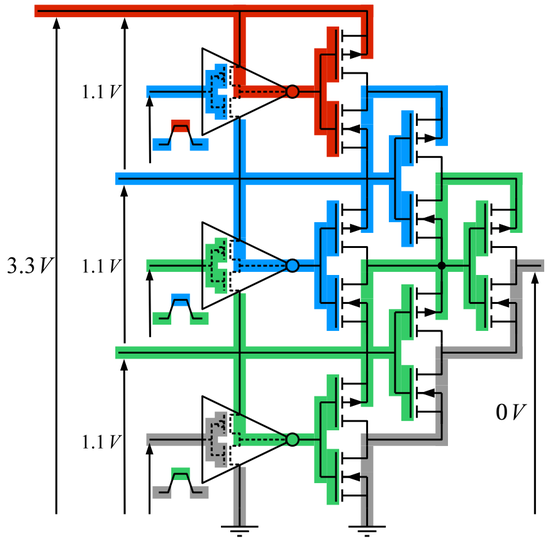
Cascoded power stage

0 V 1.1 V 2.2 V 3.3 V

Phase 1



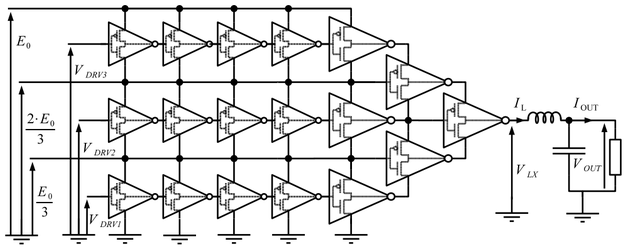
Phase 2

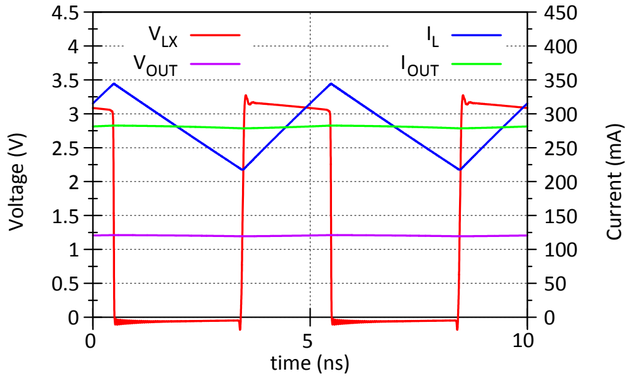


Simulation waveforms:

cascoded power stage in a 1-phase Buck

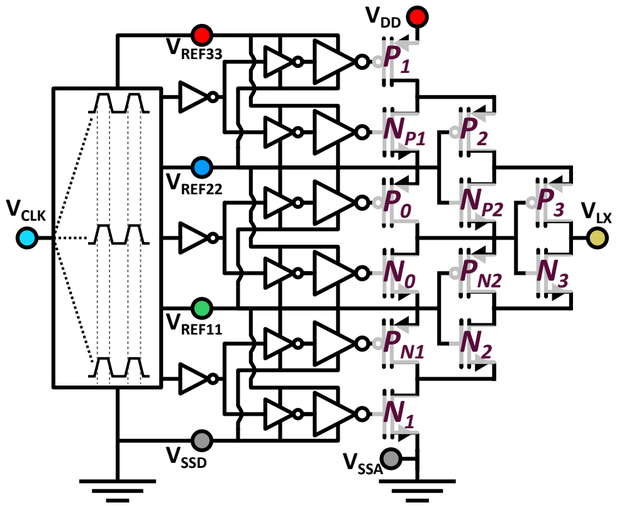
L = 30 nH; C_{OUT} = 15 nF; R_{LOAD} = 4.3 Ω; E_0 = 3.3 V



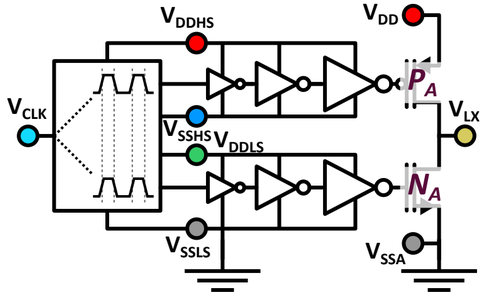


Optimization - Methodology

Cascoded converter



Standard converter



- Optimized for various configurations:
  - 200 MHz, nominal power
  - 100 MHz, half nominal power
- All transistors in cascoded power stage have a 40 nm length
- $W_{P1} = W_{P2} = W_{P3}$
- $W_{N1} = W_{N2} = W_{N3}$
- Any other width can vary independently from the others
- Driving signals are synchronized (no skew)
- Optimization also carried out on a standard power stage (3.3 V transistors), as reference
- Optimized in Cadence Virtuoso ADE-XL environment (global optimization)

Main optimization results

	Standard power stage		Cascoded power stage	
	200 MHz	100 MHz	200 MHz	100 MHz
$W_{P1,2,3}$	-	-	14.8 mm	12.4 mm
$W_{N1,2,3}$	-	-	6 mm	5.4 mm
W_{PA}	10.2 mm	7.3 mm	-	-
W_{NA}	7.7 mm	4.8 mm	-	-

Efficiency results

	Standard power stage		Cascoded power stage	
	200 MHz	100 MHz	200 MHz	100 MHz
P_{OUT}	336 mW	168 mW	336 mW	168 mW
Efficiency	80.06 %	85.9 %	88.1 %	**92.05 %**

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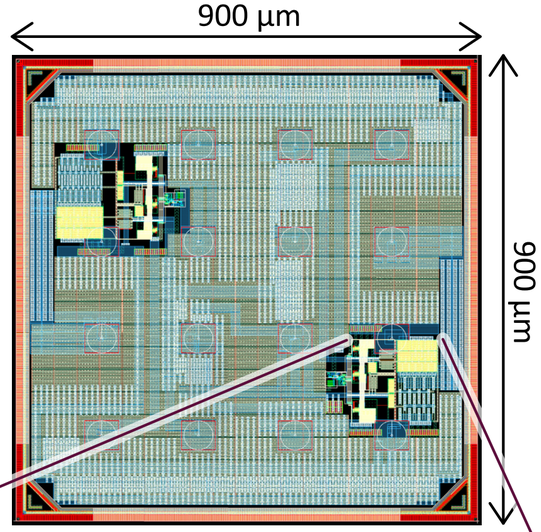
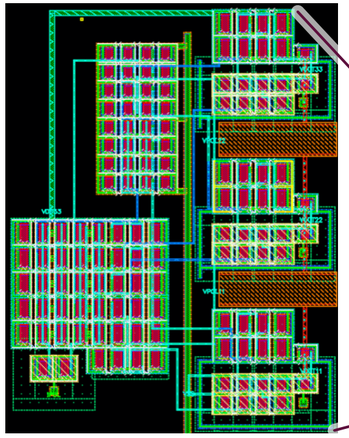
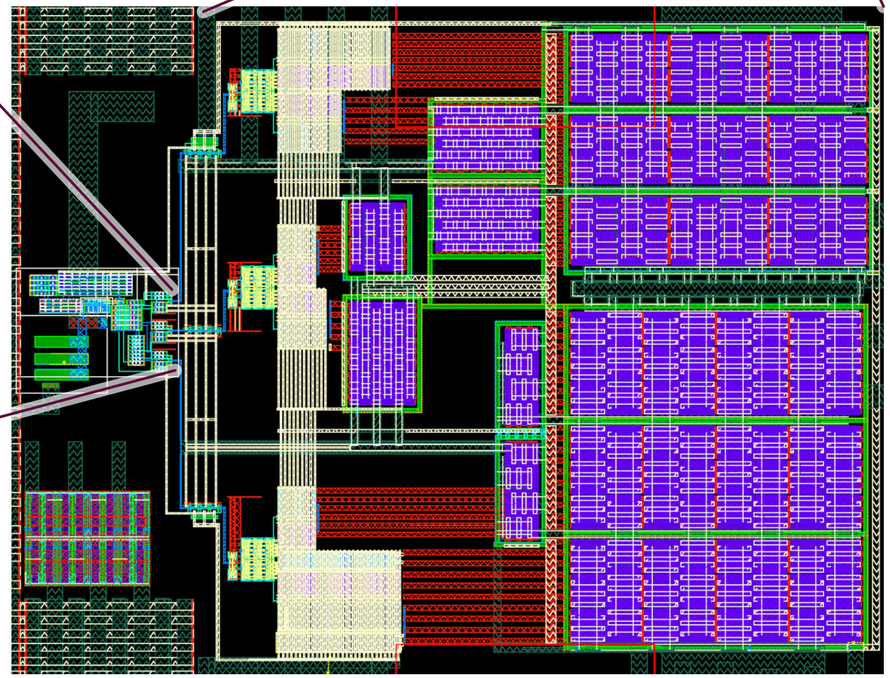
Implementation - Layout

Full chip

- 2 converters included
  - 200 MHz / 336 mW
  - 100 MHz / 168 mW
- 2 x 8 pads:
  - 1 input power (3.3 V)
  - 3 reference / polarization voltages (1.1, 2.2 and 3.3 V)
  - 1 clock signal
  - 2 grounds (for power and polarisation)
- ≈ 2 nF on-chip MOM capacitors
  - 1.1 nF for 3.3 V power
  - 3 x 0.3 nF for reference / polarization







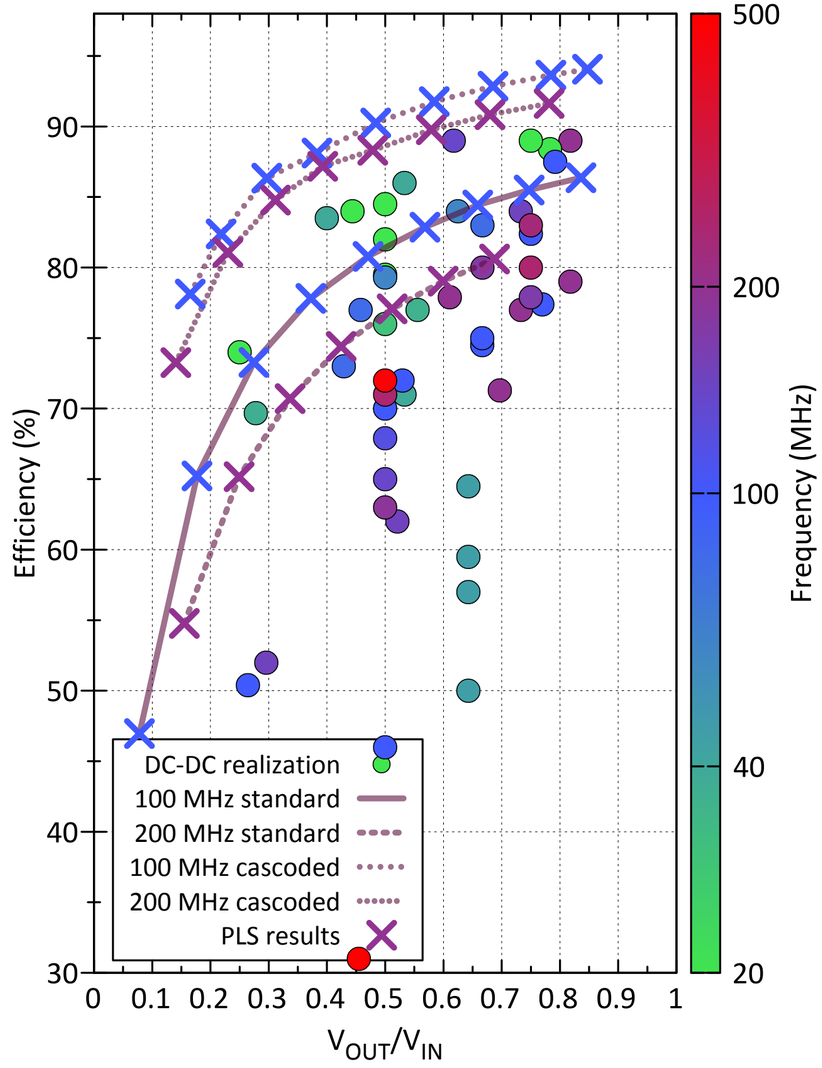
Level-shifter

- 0 - 3.3 V to 0 - 1.1 V, 1.1 - 2.2 V and 2.2 - 3.3 V
- 1.5 ns input-output delay
- 900 ps min pulse width
- 40 ps max skew
- 350 µW power comsumption

Post-layout simulation results

- Simulations made before top metal routing
- All on-chip cells are taken into account
  - Current references
  - Level shifter
  - Drivers
- Passive components losses are not simulated

- Carried out on the 4 optimized structures
- Constant input voltage: 3.3 V
- Constant output current:
  - 140 mA for 100 MHz converters
  - 280 mA for 200 MHz converters
- Varying duty-cycle



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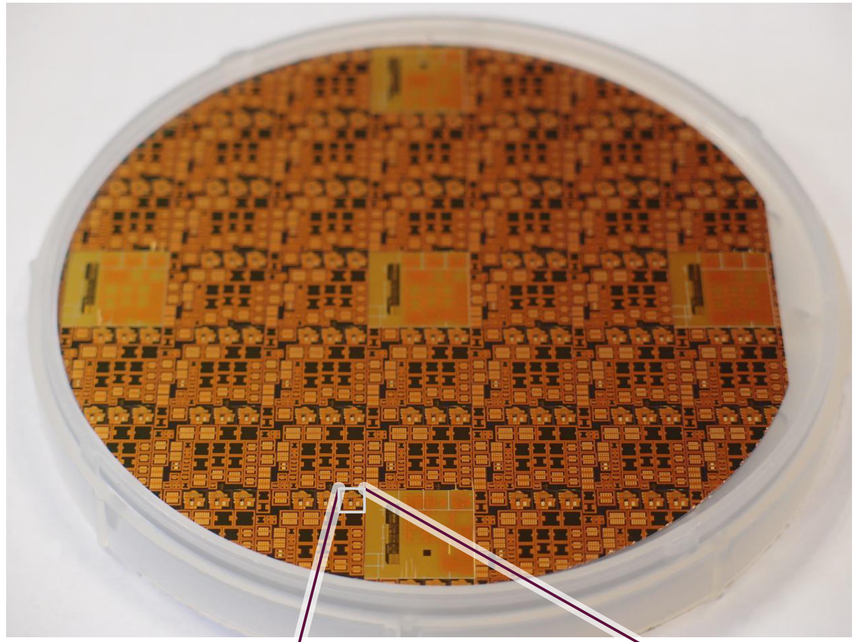
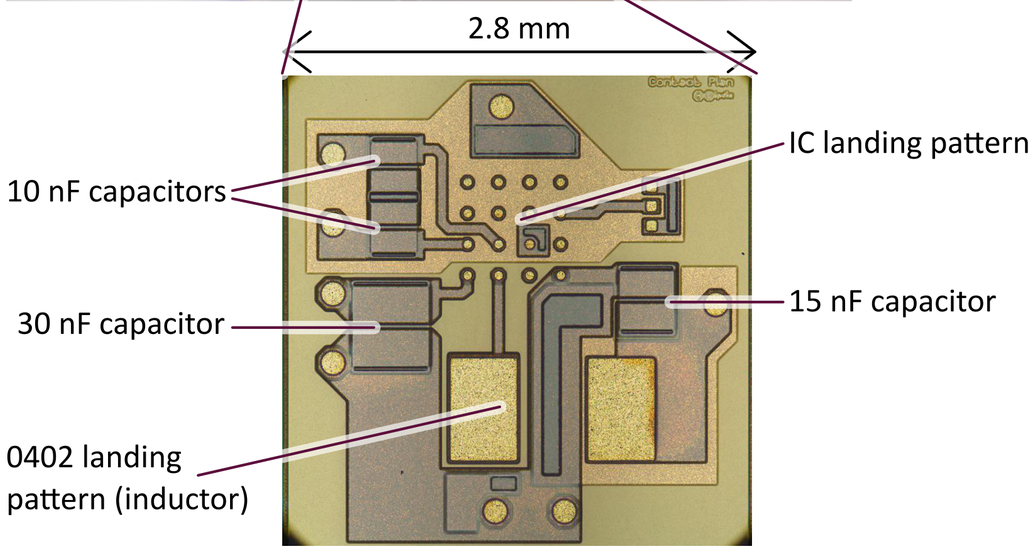
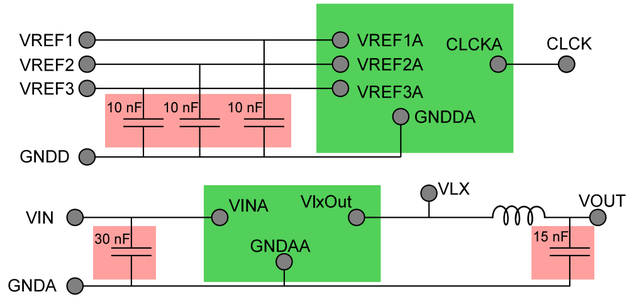
Interposer - 1st prototype





Interposer - Optimized

Interposer schematic



Main changes:

- Routing of GNDA (reducing parasitic inductance) and VLX net
- Adding VREF3 pad and its 10 nF integrated capacitor
- Adding 1 pad for tie up/down of unused IC converter